Hardware

Abstraction levels

Doped Silicon

Transistor, Resistor, Capacitor

Gate, Register, Latch (RTL)

Modules

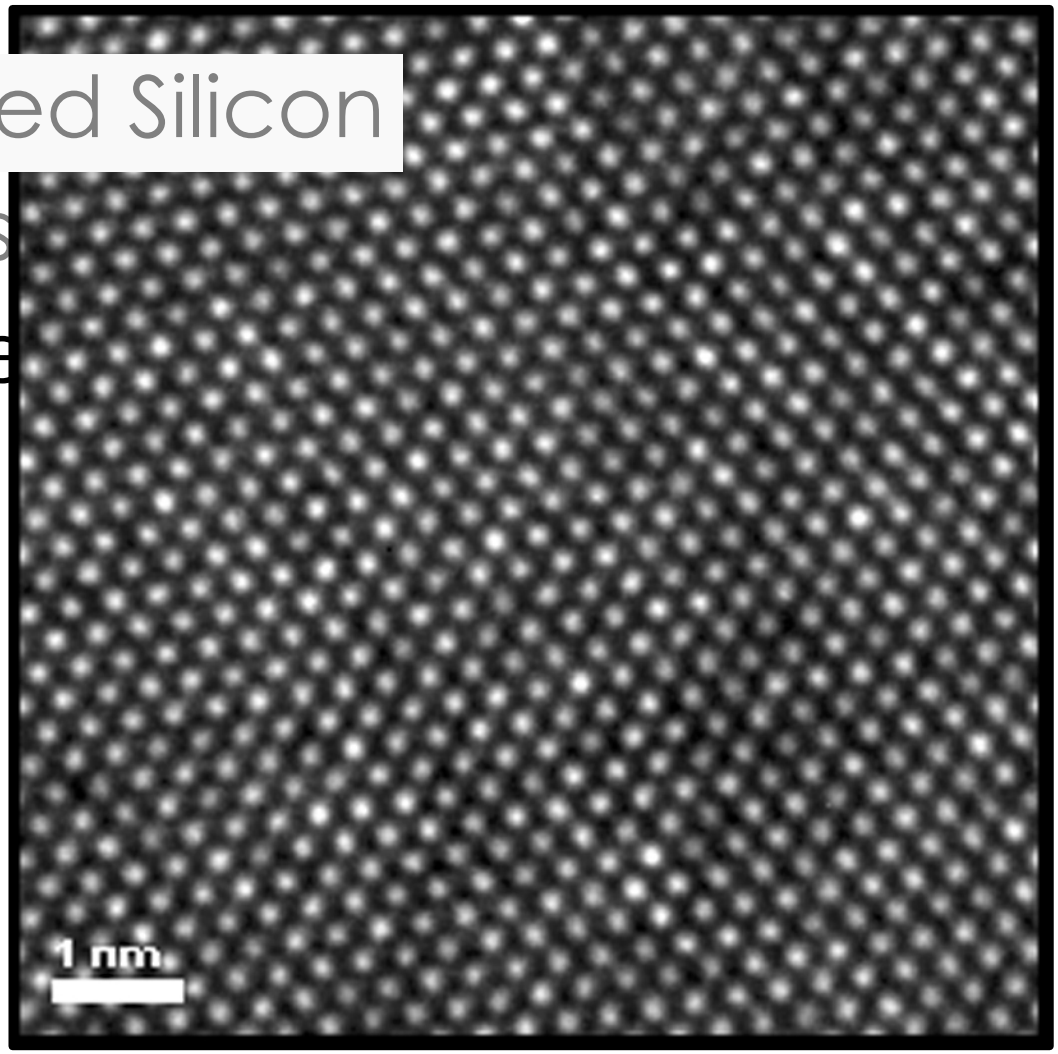
Abstraction levels

Doped Silicon

Trans

Gate

Mod



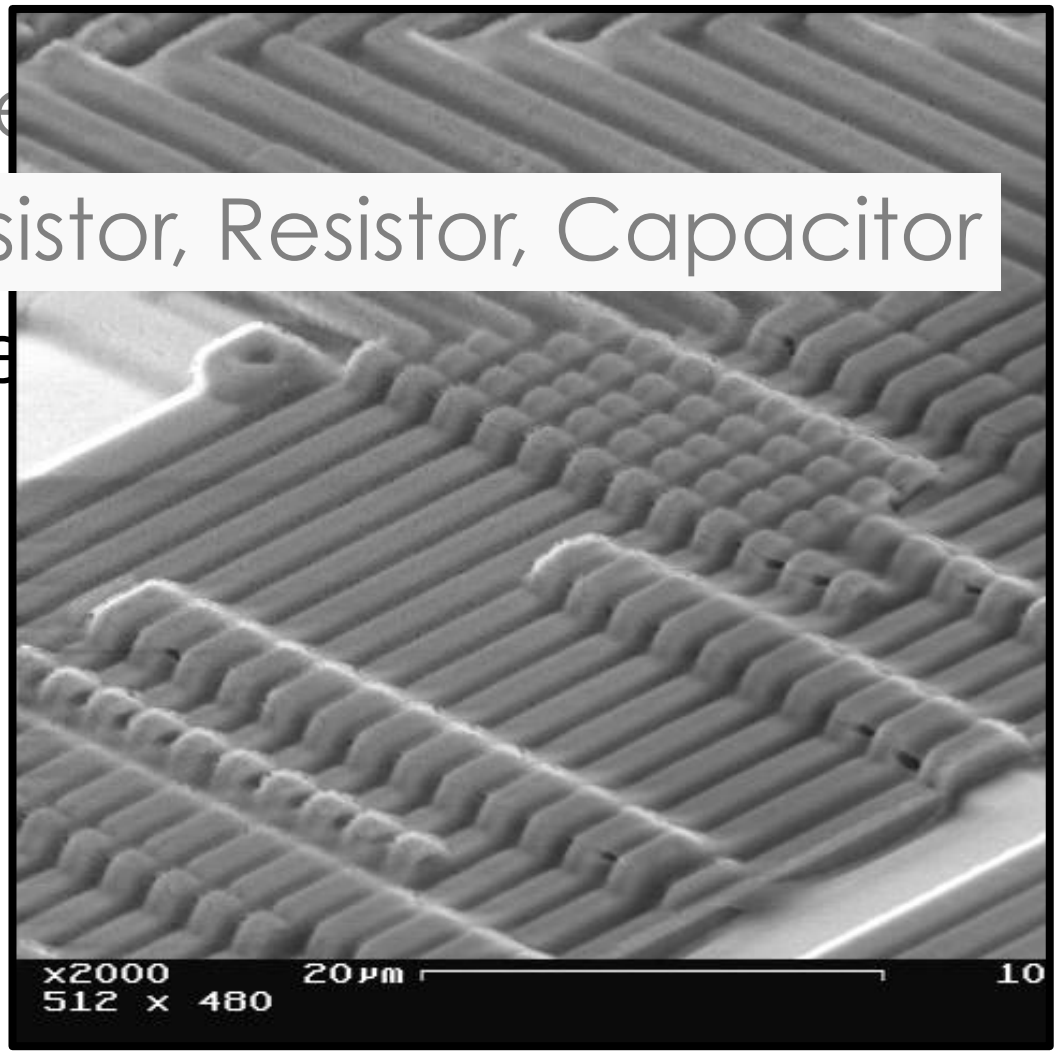
Abstraction levels

Dope

Transistor, Resistor, Capacitor

Gate

Mod



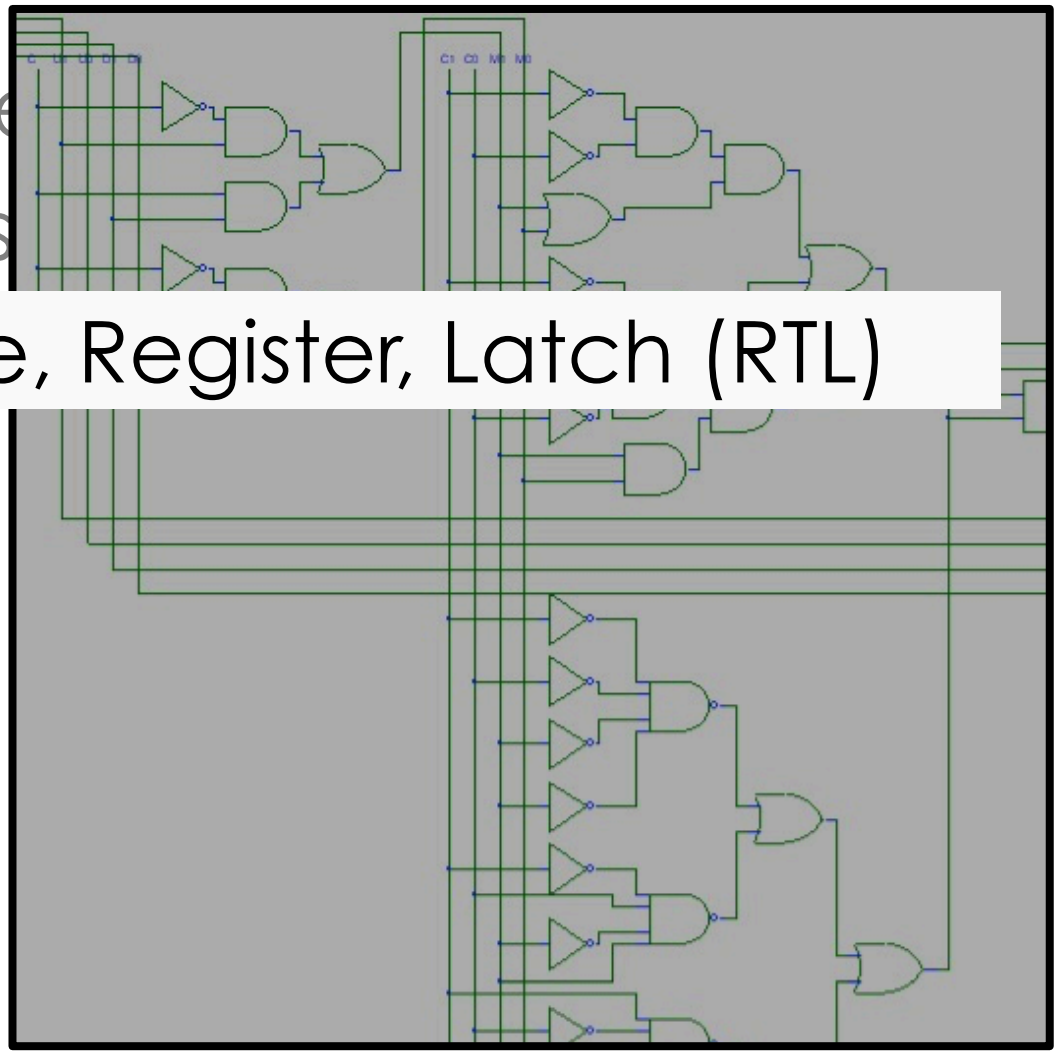
Abstraction levels

Dope

Trans

Gate, Register, Latch (RTL)

Mod



Abstraction levels

Doped Silicon

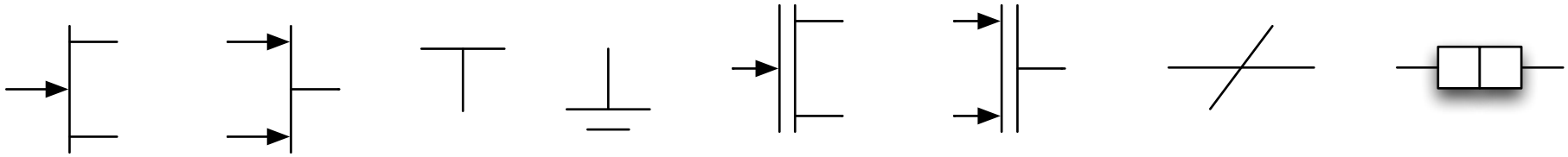
Transistor, Resistor, Capacitor

Gate, Register, Latch (RTL)

Modules

Network

8 modules: xMAS [HLDVT'10]



Results for xMAS

Verification of liveness [Verbeek'11]
Invariant generation [Chatterjee'12]
Generalization [Verbeek'12]
Type-correctness [van Gastel'14]

Invariant generation on RTL [Me'13]
Verification of liveness on RTL [Me'14]
Generating xMAS from RTL [Me'15]

Identify the interface

References

- [Chatterjee'12] S. Chatterjee and M. Kishinevsky **Automatic generation of inductive invariants from high-level microarchitectural models of communication fabrics** *Formal Methods in System Design* **40** 147--169 (2012)
- [van Gastel'14] B. van Gastel and F. Verbeek and J. Schmaltz **Inference of channel types in micro-architectural models of on-chip communication networks** (2014)
- [Me'13] S. J. C. Joosten and J. Schmaltz **Generation of inductive invariants from register transfer level designs of communication fabrics** (MemoCODE'13) 57--64 (2013)
- [Me'14] S. J. C. Joosten and J. Schmaltz **Scalable liveness verification for communication fabrics** Design automation and test Europe (DATE'14) (2014)
- [Me'15] S. J. C. Joosten and J. Schmaltz **Automatic extraction of micro-architectural models of communication fabrics from register transfer level designs**
- Design automation and test Europe (DATE'15) 1413--1418 (2015)
- [Verbeek'11] F. Verbeek and J. Schmaltz **Hunting deadlocks efficiently in microarchitectural models of communication fabrics** 223--231 (FMCAD'11) (2011)
- [Verbeek'12] F. Verbeek and J. Schmaltz **Automatic generation of deadlock detection algorithms for a family of micro architectural description languages** *IEEE International High Level Design Validation and Test Workshop (HLDVT'12)* (2012)